IN THE CLAIMS:

Please substitute the following claims for the same-numbered claims in the application:

1-7. (Cancelled).

8. (Currently Amended) A field effect transistor comprising:

a silicon substrate[[,]];

a gate stack on a top surface of said silicon substrate;

a recess in said silicon substrate at said top surface adjacent said gate stack; ~~wherein the top surface of said silicon substrate has an oxygen content comprising an amount below that which would prevent epitaxial growth;~~

an epitaxial silicon halo layer in said recess on ~~said top surface of~~ said silicon substrate; and,

an epitaxial silicon source/drain layer in said recess on said epitaxial silicon halo layer,[[;]] ~~and~~ wherein said silicon substrate comprises an oxidized portion bordering said recess directly adjacent said epitaxial silicon halo layer and wherein said oxidize portion has an oxygen content below an amount which would prevent epitaxial growth of said epitaxial silicon halo layer from said oxidized portion and further ~~a gate stack above said epitaxial silicon source/drain layer, wherein said~~ above an amount ~~of said oxygen content further~~ required to substantially limit[[s]] dopants within said epitaxial silicon halo layer and said eptiaxial silicon source/drain layer from moving into said silicon substrate.

9. (Original) The field effect transistor in claim 8, wherein source/drain dopants are substantially limited to said epitaxial silicon source/drain layer.

10. (Cancelled).

11. (Currently Amended) The field effect transistor in claim 8, wherein said silicon substrate includes a column portion ~~extending through~~ adjacent said epitaxial silicon halo layer and said epitaxial silicon source/drain layer, wherein said column portion is below said gate stack.

12. (Previously Presented) The field effect transistor in claim 9, wherein halo dopants are substantially limited to said epitaxial silicon halo layer and wherein said halo dopants are different from said source/drain dopants.

13. (Original) The field effect transistor in claim 8, further comprising isolation regions in said epitaxial silicon layer and said silicon substrate.

14. (Previously Presented) The field effect transistor in claim 8, wherein said top surface is essentially damage and native oxide free.

15-34. (Canceled).

35. (Currently Amended) A field effect transistor comprising:

a silicon substrate[[,]]~~wherein the top surface of said silicon substrate has an oxygen content comprising an amount below that which would prevent epitaxial growth from said silicon substrate~~; and

an epitaxial silicon layer directly on ~~said~~ a top surface of said silicon substrate, grown from said silicon substrate and comprising dopants,

wherein said silicon substrate comprises an oxidized portion directly adjacent said epitaxial silicon layer and wherein said oxidized portion has an oxygen content below an amount which would prevent epitaxial growth of said epitaxial silicon layer from said oxidized portion and further above an amount required to ~~wherein said dopants are~~ substantially limit~~ed to~~ said dopants within said epitaxial silicon layer ~~by said amount of said oxygen content of said top surface of~~ from moving into said silicon substrate.

36. (Previously Presented) The field effect transistor in claim 35, wherein said dopants comprise source/drain dopants and halo dopants and wherein said source/drain dopants and said halo dopants are different.

37. (Canceled).

38. (Previously Presented) The field effect transistor in claim 35, wherein said epitaxial silicon layer comprises an in-situ doped epitaxial silicon layer.

39. (Previously Presented) The field effect transistor in claim 35, further comprising source/drain regions in said epitaxial silicon layer.

40. (Previously Presented) The field effect transistor in claim 35, further comprising isolation regions in said epitaxial silicon layer and said silicon substrate.

41. (Previously Presented) The field effect transistor in claim 35, wherein said top surface is essentially damage and native oxide free.

42. (Currently Amended) A field effect transistor comprising:

a silicon substrate[[,]];

a gate stack on a top surface of said silicon substrate;

a recess in said silicon substrate at said top surface adjacent said gate stack; and

~~wherein the top surface of said silicon substrate has an oxygen content comprising an amount below that which would prevent epitaxial growth from said silicon substrate;~~

an epitaxial silicon ~~source/drain~~ layer ~~directly~~ in said recess on ~~said top surface of~~ said silicon substrate, grown from said silicon substrate and comprising ~~source/drain~~ dopants,

wherein said silicon substrate comprises an oxidized portion bordering said recess directly adjacent said epitaxial silicon layer and wherein said oxidized portion has an oxygen content below an amount which would prevent epitaxial growth of said epitaxial silicon layer from said oxidized portion and further above an amount required to ~~wherein said source/drain~~

~~dopants are~~ substantially limit~~ed to~~ said dopants within said epitaxial silicon ~~source/drain~~ layer ~~by said amount of said oxygen content of said top surface of~~ from moving into said silicon substrate.

43. (Canceled).

44. (Currently Amended) The field effect transistor in claim 42, wherein said silicon substrate includes a column portion ~~extending through~~ adjacent said epitaxial silicon ~~source/drain~~ layer, wherein said column portion is below said gate stack.

45. (Previously Presented) The field effect transistor in claim 42, wherein said top surface is essentially damage and native oxide free.

46. (Currently Amneded) The field effect transistor in claim 42, wherein said epitaxial silicon ~~source/drain~~ layer comprises an in-situ doped epitaxial silicon source/drain layer.

47. (Currently Amended) The field effect transistor in claim 42, further comprising isolation regions in said epitaxial silicon ~~source/drain~~ layer and said silicon substrate.